DOCKET NO. TI 37793 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Jiong-Ping Lu, et al.

Serial No.: N/A

Filed: Herewith

For: A METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE HAVING A SILICIDED GATE ELECTRODE AND A METHOD FOR MANUFACTURING AN INTEGRATED CIRCUIT THE SAME

Group No.: N/A

Examiner: N/A

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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3-26-2004 Elizabeth Shumacher
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Elizabeth Shumacher
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Sir:

INFORMATION DISCLOSURE STATEMENT

Pursuant to the duty of disclosure under 37 C.F.R. § 1.56, Applicant submits this statement. This submittal is made in accordance with 37 C.F.R. §§ 1.97 and 1.98 and § 609 of the Manual of Patent Examining Procedure. The patents, publications and other information herein are listed below and on the attached Form PTO-1449. Copies of the listed references are submitted herewith.

References:
Jakub Kedzierski, et al.; "ISSUES IN NiSi-GATED FDSOI DEVICE INTEGRATION"; 2003 IEEE.

Applicant hereby expressly reserves the right to swear behind the effective dates of any of the above Patents and to question the relevance and materiality of the Patents and Publications listed herein, in whole, in part, or in combination, subsequent to filing this Information Disclosure Statement. The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 20-0668.

Respectfully submitted,

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	N/A
Filing Date	Herewith
First Named Inventor	Jiong-Ping Lu, et al.
Art Unit	N/A
Examiner Name	N/A
Attorney Docket Number	TI 37793

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Jakub Kedzierski, et al.; "ISSUES IN NiSi-GATED FDSOI DEVICE INTEGRATION"; 2003 IEEE.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.